

Form PTO-1449 (modified)		Atty. Docket No. 2000.093282/TT5101D	Serial No. Unknown
List of Patents and Publications for Applicant's INFORMATION DISCLOSURE STATEMENT  (Use several sheets if necessary)		Applicant Andy C. Wei, Derick J. Wristers and Mark S. Fuselier	
		Filing Date: March 9, 2004	Group: Unknown
U.S. Patent Documents See Page 1	Foreign Patent Documents See Page 1	Other Art See Page 1	

## U.S. Patent Documents

Exam. Init.	Ref. Des.	Document Number	Date	Name	Class	Sub Class	Filing Date of App.
SDF	A1	5,482,871	01-1996	Pollack	438	151	
	A2	5,926,703	07-1999	Yamaguchi <i>et al.</i>	438	163	
	A3	6,232,163	05-2001	Voldman <i>et al.</i>	438	212	
	A4	6,352,882	03-2002	Assaderaghi <i>et al.</i>	438	155	
	A5	6,407,428	06-2002	Krishnan <i>et al.</i>	257	347	

## Foreign Patent Documents

Exam. Init.	Ref. Des.	Document Number	Date	Country	Class	Sub Class	Translation Yes/No
	B1						
	B2						
	B3						

## Other Art (Including Author, Title, Date Pertinent Pages, Etc.)

Exam. Init.	Ref. Des.	Citation
SDF	C1	Baine <i>et al.</i> , "Back Gate Effects in N-Channel Monocrystalline Silicon Devices-on-Glass and Their Suppression by Boron Ion Implantation," <i>Mat. Res. Soc. Symp. Proc.</i> , 558:369-74, 2000
	C2	Chang <i>et al.</i> , "Efficacy of Air in Reducing the Kink Effect on Floating-Body NFD/SOI CMOS," <i>Proc. 1998 IEEE Int'l SOI Conf.</i> , pp. 155-56, 1998
	C3	Ko <i>et al.</i> , "Suppression of Floating Body Effect with SIGE Source Structure for Fully Depleted SOI MOSFET's," <i>Electrochem. Soc. Proc.</i> , 2001-3:239-44, 2001
	C4	Leung <i>et al.</i> , "High voltage, high speed lateral IGBT in thin SOI for power IC," <i>SOI 1996 Int'l Conference Proceedings</i> , pp. 132-133, 1996.

EXAMINER:

Stanley Baer

DATE CONSIDERED:

02/13/04

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